19-1328; Rev 6; 3/12

Low-Voltage, CMOS Analog Multiplexers/Switches

General Description

The MAX4581/MAX4582/MAX4583 are low-voltage, CMOS analog ICs configured as an 8-channel multiplexer (MAX4581), two 4-channel multiplexers (MAX4582), and three single-pole/double-throw (SPDT) switches (MAX4583).

These CMOS devices can operate continuously with ±2V to ±6V dual power supplies or a +2V to +12V single supply. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA at +25°C or 5nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V or dual ±5V supplies.

Applications

Battery-Operated Equipment

Audio and Video Signal Routing

Low-Voltage Data-Acquisition Systems

Communications Circuits

Automotive

Features

- ♦ **MAX4582 Available in AEC-Q100 Qualified Version**
- ♦ **Offered in Automotive Temperature Range (-40°C to +125°C)**
- ♦ **Guaranteed On-Resistance**
  80Ω with ±5V Supplies
  150Ω with Single +5V Supply
- ♦ **Guaranteed On-Resistance Match Between Channels**
- ♦ **Guaranteed Low Off-Leakage Current 1nA at +25°C**
- ♦ **Guaranteed Low On-Leakage Current 1nA at +25°C**
- ♦ **+2V to +12V Single-Supply Operation**
  ±2V to ±6V Dual-Supply Operation
- ♦ **TTL/CMOS-Logic Compatible**
- ♦ **Low Distortion: < 0.02% (600Ω)**
- ♦ **Low Crosstalk: < -96dB (50Ω, MAX4582)**
- ♦ **High Off-Isolation: < -74dB (50Ω)**

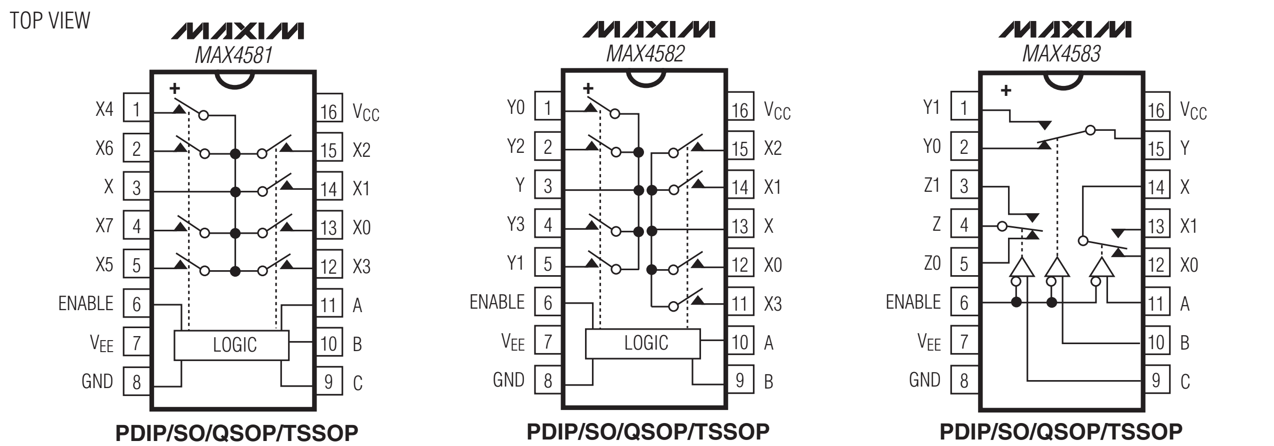
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4581CPE+	0°C to +70°C	16 PDIP	—
MAX4581CSE+	0°C to +70°C	16 Narrow SO	—
MAX4581CUE+	0°C to +70°C	16 TSSOP	—

+Denotes a lead(Pb)-free/RoHS-compliant package.

Ordering Information continued at end of data sheet.

Pin Configurations/Functional Diagrams



Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V_{EE}
V_{CC} .... -0.3V to 13V
Voltage into Any Terminal (Note 1) ...(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Continuous Current into Any Terminal ....±20mA
Peak Current, X_, Y_, Z_
(pulsed at 1ms, 10% duty cycle) ....±40mA
ESD per Method 3015.7 ....>2000V
Continuous Power Dissipation (T_A = +70°C)
16-Pin PDIP (derate 10.53mW/°C above +70°C)............842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin QSOP (derate 8.3mW/°C above +70°C)..............667mW
16-Pin TSSOP (derate 9.4mW/°C above +70°C) 755mW
16-Pin TQFN (derate 14.7mW/°C above +70°C) 1177mW
Operating Temperature Ranges
MAX458_C_ ....0°C to +70°C
MAX458_E_ ....-40°C to +85°C
MAX458_A_...-40°C to +125°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: Voltages exceeding V_{CC} or V_{EE} on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V_{CC} = 4.5V to 5.5V, V_{EE} = -4.5V to -5.5V, $V_{_H}$ = 2.4V, $V_{_L}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog-Signal Range	V_X, V_Y, V_Z			C, E, A	V_{EE}		V_{CC}	V
Switch On-Resistance	R_{ON}	V_{CC} = 4.5V; V_{EE} = -4.5V; I_X, I_Y, I_Z = 1mA; V_X, V_Y, V_Z = 3.5V		+25°C		50	80	Ω
				C, E, A			100	
Switch On-Resistance Match Between Channels (Note 3)	ΔR_{ON}	V_{CC} = 4.5V; V_{EE} = -4.5V; I_X, I_Y, I_Z = 1mA; V_X, V_Y, V_Z = 3.5V		+25°C		1	4	Ω
				C, E, A			6	
Switch On-Resistance Flatness (Note 4)	$R_{FLAT(ON)}$	V_{CC} = 5V; V_{EE} = -5V; I_X, I_Y, I_Z = 1mA; V_X, V_Y, V_Z = 3V, 0V, -3V		+25°C		4	10	Ω
				C, E, A			12	
X_, Y_, Z_ Off-Leakage (Note 5)	$I_{X_(OFF)}$, $I_{Y_(OFF)}$, $I_{Z_(OFF)}$	V_{CC} = 5.5V; V_{EE} = -5.5V; $V_{X_}$, $V_{Y_}$, $V_{Z_}$ = ±4.5V; V_X, V_Y, V_Z = ∓4.5V		+25°C	-1		+1	nA
				C, E, A	-10		+10	
X, Y, Z Off-Leakage (Note 5)	$I_{X(OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	V_{CC} = 5.5V; V_{EE} = -5.5V; $V_{X_}$, $V_{Y_}$, $V_{Z_}$ = ±4.5V; V_X, V_Y, V_Z = ∓4.5V	MAX4581	+25°C	-2		+2	nA
				C, E, A	-100		+100	
			MAX4582 MAX4583	+25°C	-1		+1	
				C, E, A	-50		+50	
X, Y, Z On-Leakage (Note 5)	$I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V_{CC} = 5.5V; V_{EE} = -5.5V; V_X, V_Y, V_Z = ±4.5V	MAX4581	+25°C	-2		+2	nA
				C, E, A	-100		+100	
			MAX4582 MAX4583	+25°C	-1		+1	
				C, E, A	-50		+50	
DIGITAL I/O								
Logic Input Logic Threshold High	V_{AH}, V_{BH}, V_{CH}			C, E, A		1.5	2.4	V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, V_{CL}			C, E, A	0.8	1.5		V

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V_{CC} = 4.5V to 5.5V, V_{EE} = -4.5V to -5.5V, $V_{_H}$ = 2.4V, $V_{_L}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP (Note 2)	MAX	UNITS
Input-Current High	I_{AH}, I_{BH}, I_{CH}	V_A, V_B, V_C = 2.4V		C, E, A	-1		+1	µA
Input-Current Low	I_{AL}, I_{BL}, I_{CL}	V_A, V_B, V_C = 0.8V		C, E, A	-1		+1	µA
SWITCH DYNAMIC CHARACTERISTICS								
Inhibit Turn-On Time	$t_{(ON)}$	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 3V; R_L = 300Ω; C_L = 35pF; Figure 3		T_A = +25°C		100	200	ns
				C, E, A			200	
Inhibit Turn-Off Time	$t_{(OFF)}$	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 3V; R_L = 300Ω; C_L = 35pF; Figure 3		T_A = +25°C		40	100	ns
				C, E, A			150	
Address Transition Time	t_{TRANS}	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = ±3V; R_L = 300Ω; C_L = 35pF; Figure 2		T_A = +25°C		90	200	ns
				C, E, A			200	
Break-Before-Make Time	t_{BBM}	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 3V; R_L = 300Ω; C_L = 35pF; Figure 4		T_A = +25°C	4	20		ns
Charge Injection (Note 6)	Q	C = 1nF, R_S = 0Ω, V_S = 0V		T_A = +25°C		0.5	5	pC
Input Off-Capacitance	$C_{X_(OFF)}$, $C_{Y_(OFF)}$, $C_{Z_(OFF)}$	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 0V; f = 1MHz; Figure 7		T_A = +25°C		4		pF
Output Off-Capacitance	$C_{X(OFF)}$, $C_{Y(OFF)}$, $C_{Z(OFF)}$	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 0V; f = 1MHz; Figure 7	MAX4581	T_A = +25°C		18		pF
			MAX4582			10		
			MAX4583			6		
Output On-Capacitance	$C_{X(ON)}$, $C_{Y(ON)}$, $C_{Z(ON)}$	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 0V; f = 1MHz; Figure 7	MAX4581	T_A = +25°C		25		pF
			MAX4582			17		
			MAX4583			12.5		
Off-Isolation	V_{ISO}	R_L = 50Ω, f = 1MHz, Figure 6		T_A = +25°C		-74		dB
Channel-to-Channel Crosstalk	V_{CT}	R_L = 50Ω, f = 1MHz, Figure 6	MAX4581	T_A = +25°C		-78		dB
			MAX4582	T_A = +25°C		-96		
			MAX4583	T_A = +25°C		-73		pF
Total Harmonic Distortion	THD	R_L = 600Ω, 5Vp-p, f = 20Hz to 20kHz		T_A = +25°C		0.02		%
POWER SUPPLY								
Power-Supply Range	V_{CC}, V_{EE}			C, E, A	±2		±6	V
Power-Supply Current	I_{CC}, I_{EE}	V_{CC} = 5.5V, V_{EE} = -5.5V, V_A, V_B, V_C, V_{Enable} = V+ or 0V		T_A = +25°C	-1		+1	µA
				C, E, A	-10		+10	

Low-Voltage, CMOS Analog Multiplexers/Switches

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V_{CC} = 4.5V to 5.5V, V_{EE} = 0V, $V_{_H}$ = 2.4V, $V_{_L}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog-Signal Range	$V_{X_}$, $V_{Y_}$, $V_{Z_}$, V_X, V_Y, V_Z			C, E, A	V_{EE}		V_{CC}	V
Switch On-Resistance	R_{ON}	V_{CC} = 4.5V; I_X, I_Y, I_Z = 1mA; V_X, V_Y, V_Z = 3.5V		T_A = +25°C		90	150	Ω
				C, E, A			200	
Switch On-Resistance Match Between Channels (Note 3)	ΔR_{ON}	V_{CC} = 4.5V; I_X, I_Y, I_Z = 1mA; V_X, V_Y, V_Z = 3.5V		T_A = +25°C		2	8	Ω
				C, E, A			10	
X_, Y_, Z Off-Leakage (Note 5)	$I_{X_(OFF)}$, $I_{Y_(OFF)}$, $I_{Z_(OFF)}$	V_{CC} = 5.5V; $V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 1V, 4.5V; V_X, V_Y, V_Z = 4.5V, 1V		T_A = +25°C	-1		+1	nA
				C, E, A	-10		+10	
X, Y, Z Off-Leakage (Note 5)	$I_{X(OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	V_{CC} = 5.5V; $V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 1V, 4.5V; V_X, V_Y, V_Z = 4.5V, 1V	MAX4581	T_A = +25°C	-2		+2	nA
				C, E, A	-100		+100	
			MAX4582 MAX4583	T_A = +25°C	-1		+1	
				C, E, A	-50		+50	
X, Y, Z On-Leakage (Note 5)	$I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V_{CC} = 5.5V; V_X, V_Y, V_Z = 4.5V, 1V	MAX4581	T_A = +25°C	-2		+2	nA
				C, E, A	-100		+100	
			MAX4582 MAX4583	T_A = +25°C	-1		+1	
				C, E, A	-50		+50	
DIGITAL I/O								
Logic Input Logic Threshold High	V_{AH}, V_{BH}, V_{CH}, $V_{ENABLEH}$			C, E, A		1.5	2.4	V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, V_{CL}, $V_{ENABLEL}$			C, E, A	0.8	1.5		V
Input-Current High	I_{AH}, I_{BH}, I_{CH}, $I_{ENABLEH}$	V_{AL}, V_{BL}, V_{CL}, $V_{EnableL}$ = 2.4V		C, E, A	-1		+1	µA
Input-Current Low	I_{AL}, I_{BL}, I_{CL}, $I_{ENABLEL}$	V_{AL}, V_{BL}, V_{CL}, $V_{EnableL}$ = 0.8V		C, E, A	-1		+1	µA
SWITCH DYNAMIC CHARACTERISTICS								
Charge Injection (Note 6)	Q	C = 1nF, R_S = 0Ω, V_S = 2.5V		T_A = +25°C		0.8	5	pC
Enable Turn-On Time	$t_{(ON)}$	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 3V, R_L = 300Ω, C_L = 35pF, Figure 3		T_A = +25°C		100	200	ns
				C, E, A			250	
Enable Turn-Off Time	$t_{(OFF)}$	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 3V, R_L = 300Ω, C_L = 35pF, Figure 3		T_A = +25°C		40	100	ns
				C, E, A			150	
Address Transition Time	t_{TRANS}	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 3V/0V, R_L = 300Ω, C_L = 35pF, Figure 2		T_A = +25°C		80	200	ns
				C, E, A			250	
Break-Before-Make Time	t_{BBM}	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 3V, R_L = 300Ω, C_L = 35pF, Figure 4		T_A = +25°C	10	30		ns
POWER SUPPLY								
Power-Supply Range	V_{CC}, V_{EE}			C, E, A	2		12	V
Power-Supply Current	I_{CC}, I_{EE}	V_{CC} = 3.6V; V_A, V_B, V_C, V_{Enable} = V+ or 0V		T_A = +25°C	-1		+1	µA
				C, E, A	-10		+10	

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V_{CC} = 2.7V to 3.6V, V_{EE} = 0V, $V_{_H}$ = 2.0V, $V_{_L}$ = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog-Signal Range	$V_{X_}$, $V_{Y_}$, $V_{Z_}$, V_X, V_Y, V_Z			C, E, A	V_{EE}		V_{CC}	V
Switch On-Resistance	R_{ON}	V_{CC} = 2.7V; I_X, I_Y, I_Z = 0.1mA; V_X, V_Y, V_Z = 1.5V		T_A = +25°C		190	450	Ω
				C, E, A			550	
X_, Y_, Z_ Off-Leakage (Note 5)	$I_{X_(OFF)}$, $I_{Y_(OFF)}$, $I_{Z_(OFF)}$	V_{CC} = 3.6V; $V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 1V, 3V; V_X, V_Y, V_Z = 3V, 1V		T_A = +25°C	-1		+1	nA
				C, E, A	-10		+10	
X, Y, Z Off-Leakage (Note 6)	$I_{X(OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	V_{CC} = 3.6V; $V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 1V, 3.0V; V_X, V_Y, V_Z = 3.0V, 1V	MAX4581	T_A = +25°C	-2		+2	nA
				C, E, A	-100		+100	
			MAX4582 MAX4583	T_A = +25°C	-1		+1	
				C, E, A	-50		+50	
X, Y, Z On-Leakage (Note 6)	$I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V_{CC} = 3.6V; V_X, V_Y, V_Z = 3.0V, 1V	MAX4581	T_A = +25°C	-2		+2	nA
				C, E, A	-100		+100	
			MAX4582 MAX4583	T_A = +25°C	-1		+1	
				C, E, A	-50		+50	
DIGITAL I/O								
Logic Input Logic Threshold High	V_{AH}, V_{BH}, V_{CH}, $V_{ENABLEH}$			C, E, A		1.0	2.0	V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, V_{CL}, $V_{ENABLEL}$			C, E, A	0.5	1.0		V
Input-Current High	I_{AH}, I_{BH}, I_{CH}, $I_{ENABLEH}$	V_A, V_B, V_C = V_{Enable} = 2.0V		C, E, A	-1		+1	µA
Input-Current Low	I_{AL}, I_{BL}, I_{CL}, $I_{ENABLEL}$	V_A, V_B, V_C = V_{Enable} = 0.5V		C, E, A	-1		+1	µA
SWITCH DYNAMIC CHARACTERISTICS (Note 6)								
Enable Turn-On Time	$t_{(ON)}$	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 1.5V; R_L = 300Ω; C_L = 35pF; Figure 3		T_A = +25°C		170	300	ns
				C, E, A			400	
Enable Turn-Off Time	$t_{(OFF)}$	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 1.5V; R_L = 300Ω; C_L = 35pF; Figure 3		T_A = +25°C		50	200	ns
				C, E, A			300	
Address Transition Time	t_{TRANS}	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 1.5V/0V; R_L = 300Ω; C_L = 35pF; Figure 2		T_A = +25°C		130	300	ns
				C, E, A			400	
Break-Before-Make Time	t_{BBM}	$V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 1.5V; R_L = 300Ω; C_L = 35pF		T_A = +25°C	15	40		ns
POWER SUPPLY								
Power-Supply Current	I_{CC}, I_{EE}	V_{CC} = 3.6V, V_A, V_B, V_C, V_{Enable} = V+ or 0V		T_A = +25°C	-1		+1	µA
				C, E, A	-10		+10	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., $V_{X_}$, $V_{Y_}$, $V_{Z_}$ = 3V to 0 and 0 to -3V.

Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.

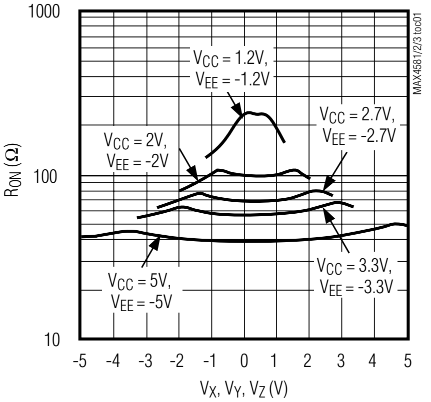
Note 6: Guaranteed by design, not production tested.

Low-Voltage, CMOS Analog Multiplexers/Switches

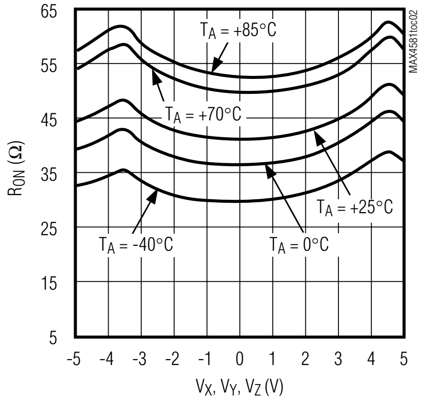
Typical Operating Characteristics

(V_{CC} = 5V, V_{EE} = -5V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted.)

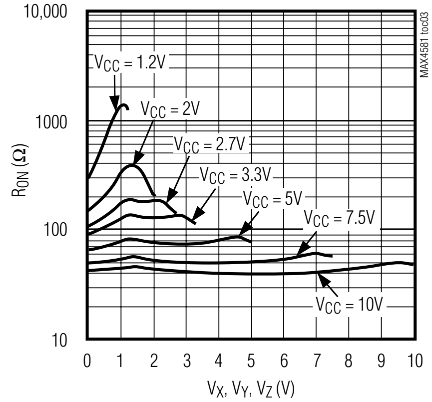
ON-RESISTANCE vs. V_X, V_Y, V_Z (DUAL SUPPLIES)



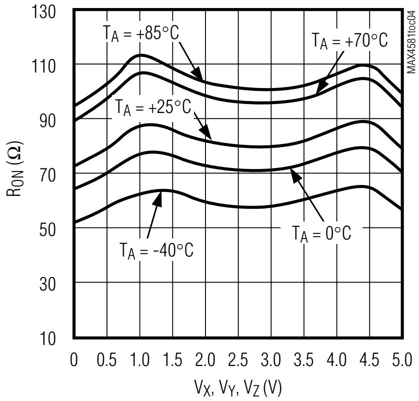
ON-RESISTANCE vs. V_X, V_Y, V_Z AND TEMPERATURE (DUAL SUPPLIES)



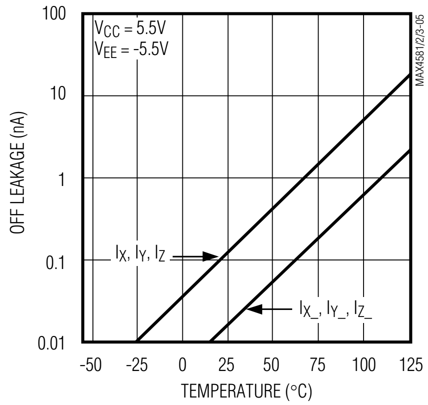
ON-RESISTANCE vs. V_X, V_Y, V_Z (SINGLE SUPPLY)



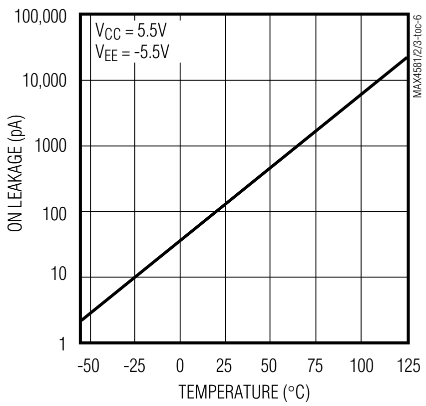
ON-RESISTANCE vs. V_X, V_Y, V_Z AND TEMPERATURE (SINGLE SUPPLY)



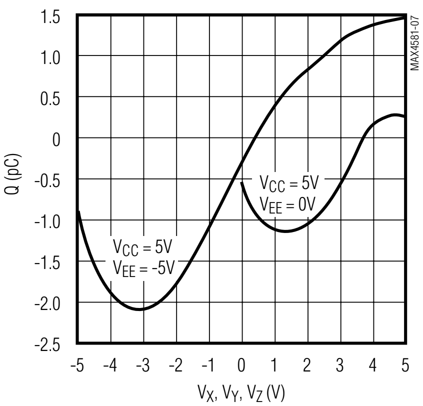
OFF-LEAKAGE vs. TEMPERATURE



ON-LEAKAGE vs. TEMPERATURE



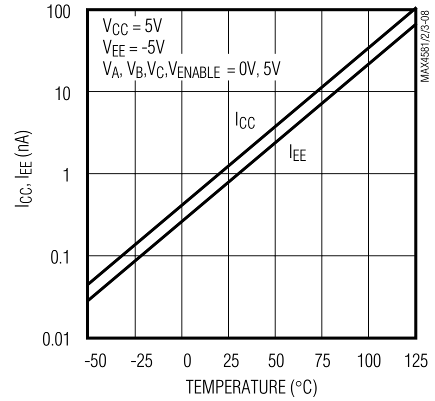
CHARGE INJECTION vs. V_X, V_Y, V_Z



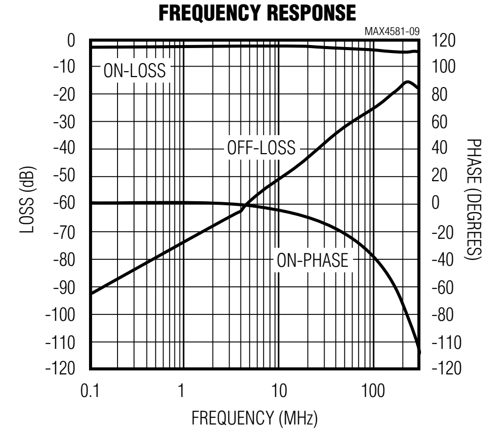
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted.)

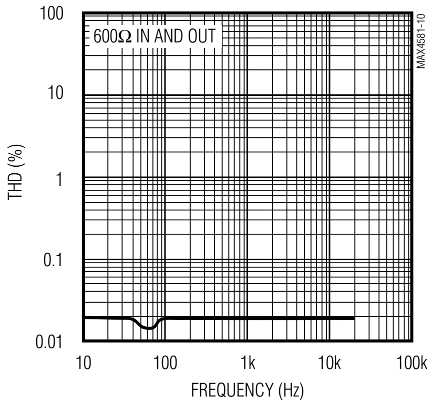
SUPPLY CURRENT vs. TEMPERATURE



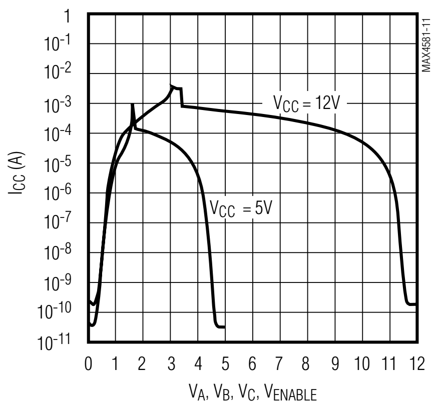
FREQUENCY RESPONSE



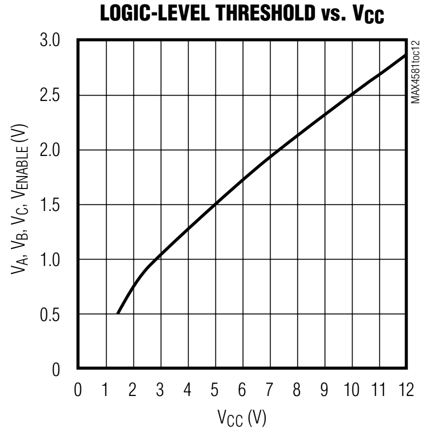
TOTAL HARMONIC DISTORTION vs. FREQUENCY



V_{CC} CURRENT vs. LOGIC LEVEL (V_A, V_B, V_C, V_{ENABLE})



LOGIC-LEVEL THRESHOLD vs. V_{CC}



Low-Voltage, CMOS Analog Multiplexers/Switches

Pin Description

PIN						NAME	FUNCTION
MAX4581		MAX4582		MAX4583			
PDIP, SO, TSSOP	TQFN-EP	PDIP, SO, TSSOP	TQFN-EP	PDIP, SO, TSSOP	TQFN-EP		
13, 14, 15, 12, 1, 5, 2, 4	11, 12, 13, 10, 15, 3, 16, 2	—	—	—	—	X0–X7	Analog Switch Inputs 0–7
3	1	13	11	14	12	X	Analog Switch “X” Output
—	—	12, 14, 15, 11	10, 12, 13, 9	—	—	X0, X1, X2, X3	Analog Switch “X” Inputs 0–3
—	—	1, 5, 2, 4	15, 3, 16, 2	—	—	Y0, Y1, Y2, Y3	Analog Switch “Y” Inputs 0–3
—	—	3	1	15	13	Y	Analog Switch “Y” Output
—	—	—	—	13	11	X1	Analog Switch “X” Normally Open Input
—	—	—	—	12	10	X0	Analog Switch “X” Normally Closed Input
—	—	—	—	1	15	Y1	Analog Switch “Y” Normally Open Input
—	—	—	—	2	16	Y0	Analog Switch “Y” Normally Open Input
—	—	—	—	3	1	Z1	Analog Switch “Z” Normally Open Input
—	—	—	—	5	3	Z0	Analog Switch “Z” Normally Open Input
—	—	—	—	4	2	Z	Analog Switch “Z” Output
16	14	16	14	16	14	V_{CC}	Positive Analog and Digital Supply-Voltage Input
11	9	10	8	11	9	A	Digital Address “A” Input
10	8	9	7	10	8	B	Digital Address “B” Input
9	7	—	—	9	7	C	Digital Address “C” Input
8	6	8	6	8	6	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V_{CC} and V_{EE}.)
7	5	7	5	7	5	V_{EE}	Negative Analog Supply-Voltage Input. Connect to GND for single-supply operation.
6	4	6	4	6	4	ENABLE	Digital Enable Input. Normally connected to GND.
—	—	—	—	—	—	EP	Exposed Pad (TQFN only). Connect EP to V_{CC}.

Note: *Input and output pins are identical and interchangeable. Any may be considered an input or output; signals pass equally well in both directions.*

Applications Information

Power-Supply Considerations

Overview

The MAX4581/MAX4582/MAX4583 construction is typical of most CMOS analog switches. They have three supply pins: V_{CC}, V_{EE}, and GND. V_{CC} and V_{EE} are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V_{CC} and V_{EE}. If any analog signal exceeds V_{CC} or V_{EE}, one of these diodes

Table 1. Truth Table/Switch Programming

ENABLE INPUT	SELECT INPUTS			ON SWITCHES		
	C*	**B**	**A**	**MAX4581**	**MAX4582**	**MAX4583**
H	X	X	X	All switches open	All switches open	All switches open
L	L	L	L	X–X0	X–X0, Y–Y0	X–X0, Y–Y0, Z–Z0
L	L	L	H	X–X1	X–X1, Y–Y1	X–X1, Y–Y0, Z–Z0
L	L	H	L	X–X2	X–X2, Y–Y2	X–X0, Y–Y1, Z–Z0
L	L	H	H	X–X3	X–X3, Y–Y3	X–X1, Y–Y1, Z–Z0
L	H	L	L	X–X4	X–X0, Y–Y0	X–X0, Y–Y0, Z–Z1
L	H	L	H	X–X5	X–X1, Y–Y1	X–X1, Y–Y0, Z–Z1
L	H	H	L	X–X6	X–X2, Y–Y2	X–X0, Y–Y1, Z–Z1
L	H	H	H	X–X7	X–X3, Y–Y3	X–X1, Y–Y1, Z–Z1

X = Don't care
**C not present on MAX4582.*
Note: *Input and output pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.*

will conduct. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V_{CC} or V_{EE}.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V_{CC} or V_{EE} and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V_{CC} and V_{EE} pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog-signal paths and GND.

V_{CC} and GND power the internal logic and logic-level translators, and set the input logic limits. The logic-level translators convert the logic levels into switched V_{CC} and V_{EE} signals to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies and signals and the analog supplies. V_{CC} and V_{EE} have ESD-protection diodes to GND.

The logic-level thresholds are TTL/CMOS compatible when V_{CC} is +5V. As V_{CC} rises, the threshold increases

slightly, so when V_{CC} reaches +12V the threshold is about 3.1V (above the TTL-guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs).

Bipolar Supplies

These devices operate with bipolar supplies between ±2V and ±5V. The V_{CC} and V_{EE} supplies need not be symmetrical, but their sum cannot exceed the +13V absolute maximum rating

Single Supply

These devices operate from a single supply between +2V and +12V when V_{EE} is connected to GND. All of the bipolar precautions must be observed. At room temperature, they actually "work" with a single supply near or below +1.7V, although as supply voltage decreases, switch on-resistance and switching times become very high.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_{CC} on first, then V_{EE}, followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with the supply pins for overvoltage protection (Figure 1).

Adding diodes reduces the analog-signal range to one diode drop below V_{CC} and one diode drop above V_{EE}, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V_{CC} and V_{EE} should not exceed 13V. These protection diodes are not recommended when using a single supply if signal levels must extend to ground.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks which are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -50dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also degrade off isolation. Adjacent channel attenuation is about 3dB above that of a bare IC socket and is entirely due to capacitive coupling.

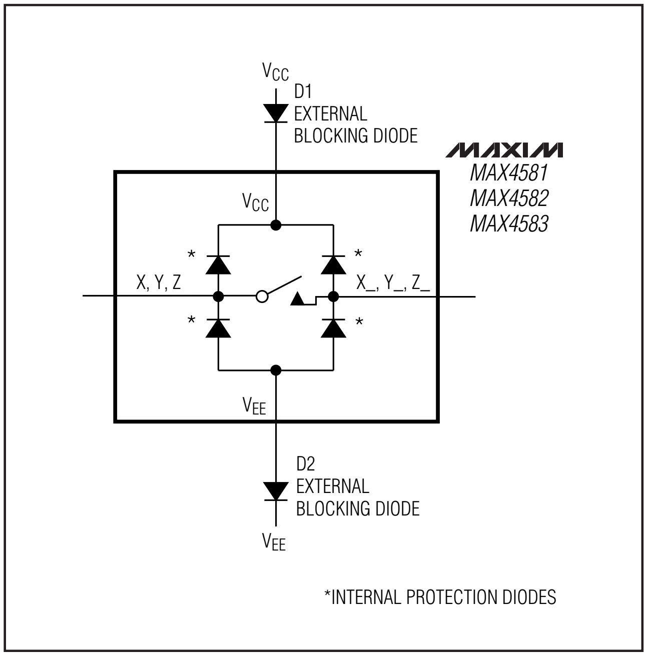


Figure 1. Overvoltage Protection Using External Blocking Diodes

Pin Nomenclature

The MAX4581/MAX4582/MAX4583 are pin-compatible with the industry-standard 74HC4051/74HC4052/74HC4053 and the MAX4051/MAX4052/MAX4053. They function identically and have identical logic diagrams, although these parts differ electrically.

The pin designations and logic diagrams in this data sheet conform to the original 1972 specifications published by RCA for the CD4051/CD4052/CD4053. These designations differ from the standard Maxim switch and mux designations as found all other Maxim data sheets (including the MAX4051/MAX4052/MAX4053) and may cause confusion. Designers who feel more comfortable with Maxim's standard designations are advised that the pin designations and logic diagrams on the MAX4051/MAX4052/MAX4053 data sheet may be freely applied to the MAX4581/MAX4582/MAX4583.

Test Circuits/Timing Diagrams

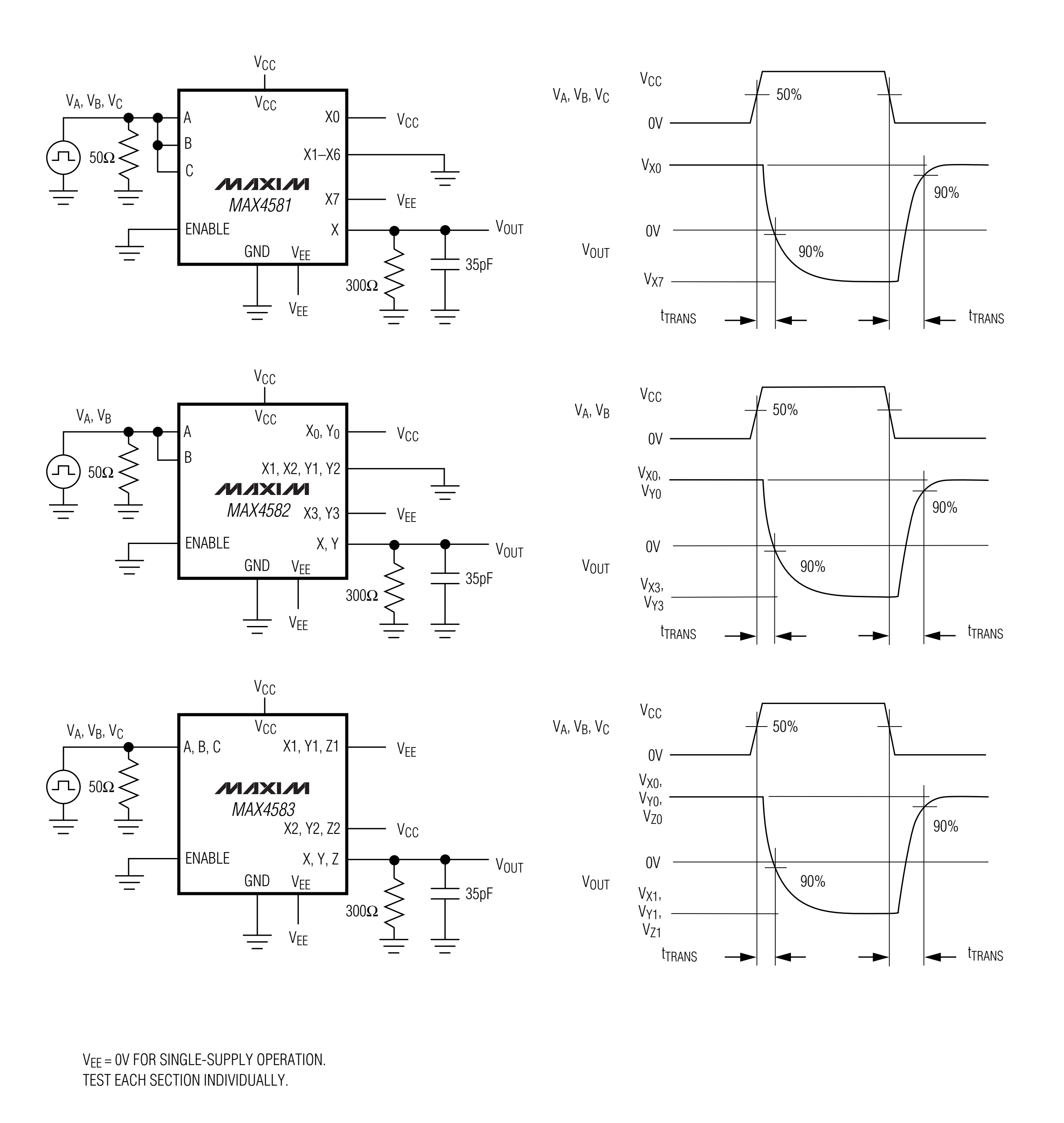
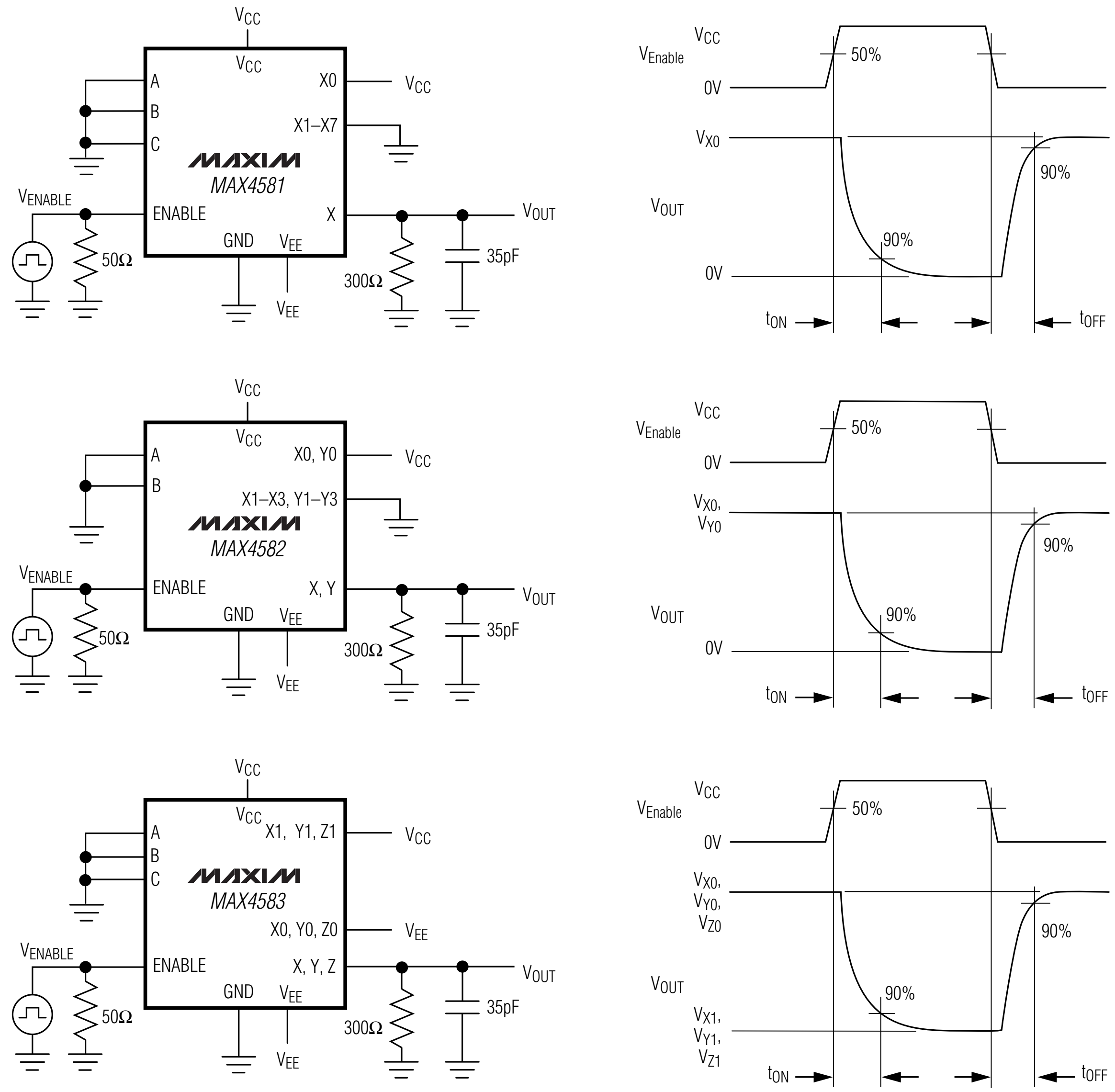


Figure 2. Address Transition Times

Low-Voltage, CMOS Analog Multiplexers/Switches

Test Circuits/Timing Diagrams (continued)



V_{EE} = 0V FOR SINGLE-SUPPLY OPERATION.
TEST EACH SECTION INDIVIDUALLY.

Figure 3. Inhibit Switching Times

Test Circuits/Timing Diagrams (continued)

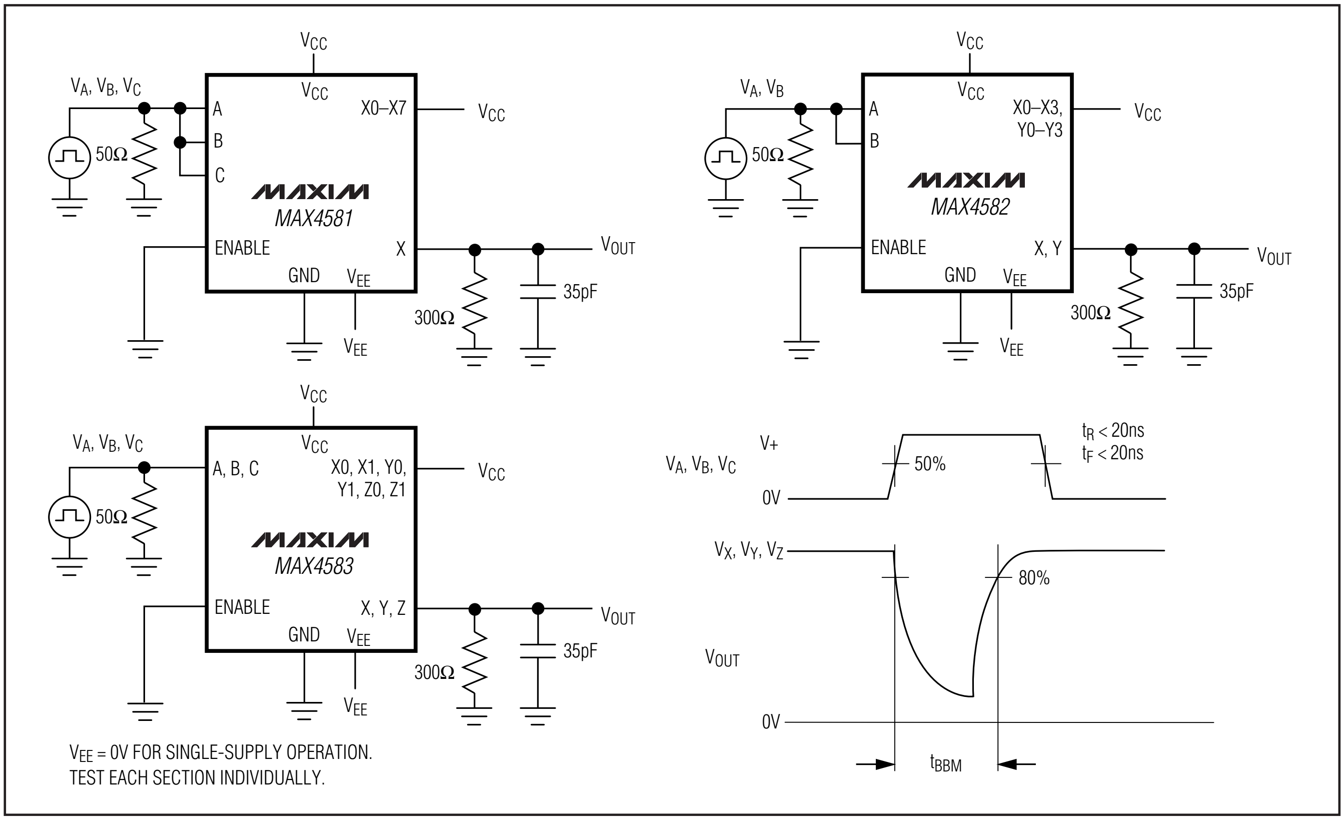


Figure 4. Break-Before-Make Interval

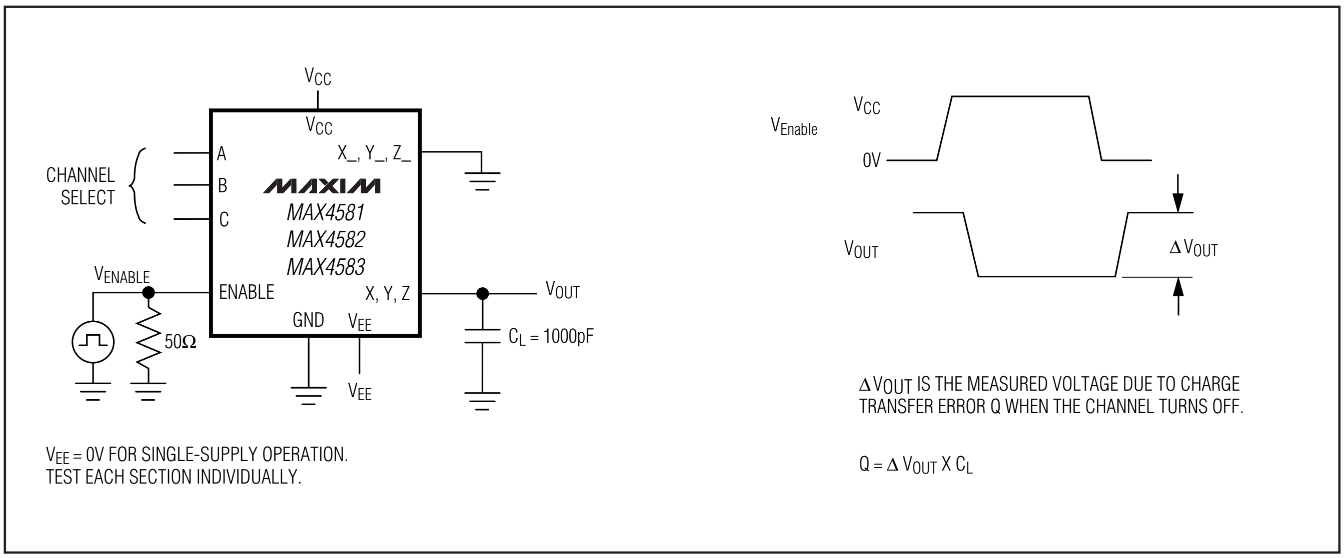
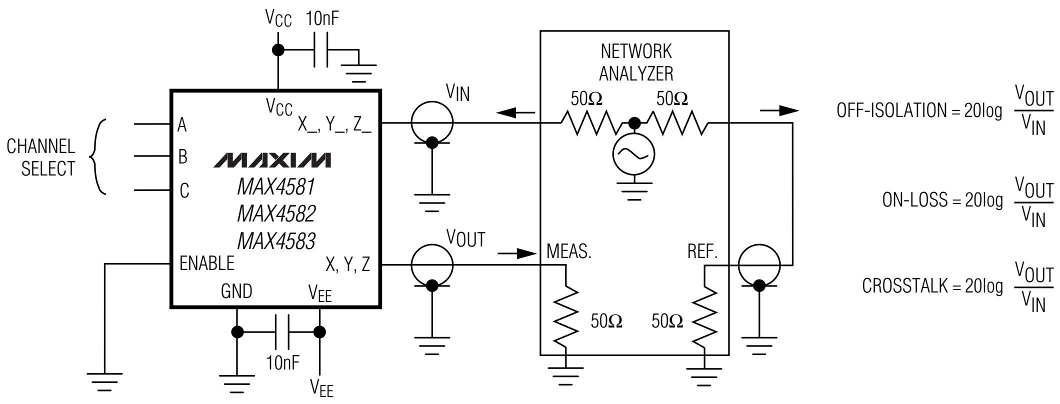


Figure 5. Charge Injection

Test Circuits/Timing Diagrams (continued)



MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
OFF-ISOLATION IS MEASURED BETWEEN COM AND "OFF" NO TERMINAL ON EACH SWITCH.
ON-LOSS IS MEASURED BETWEEN COM AND "ON" NO TERMINAL ON EACH SWITCH.
CROSSTALK (MAX4582/MAX4583) IS MEASURED FROM ONE CHANNEL (A, B, C) TO ALL OTHER CHANNELS.
SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

Figure 6. Off Isolation, On Loss, and Crosstalk

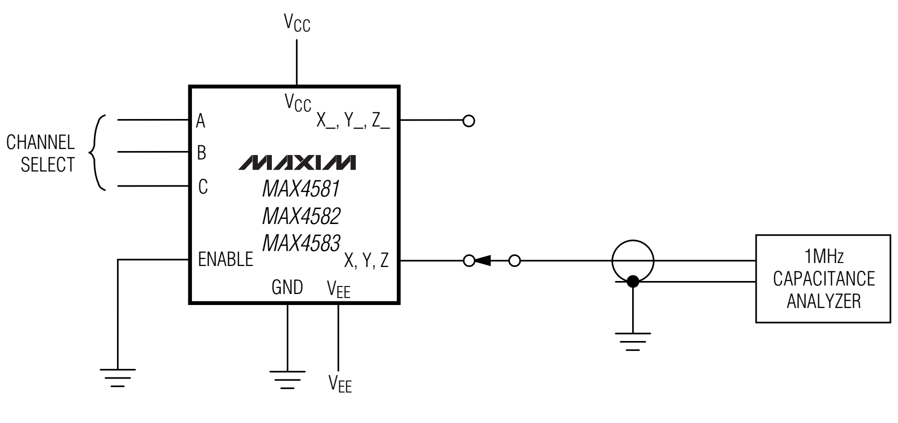
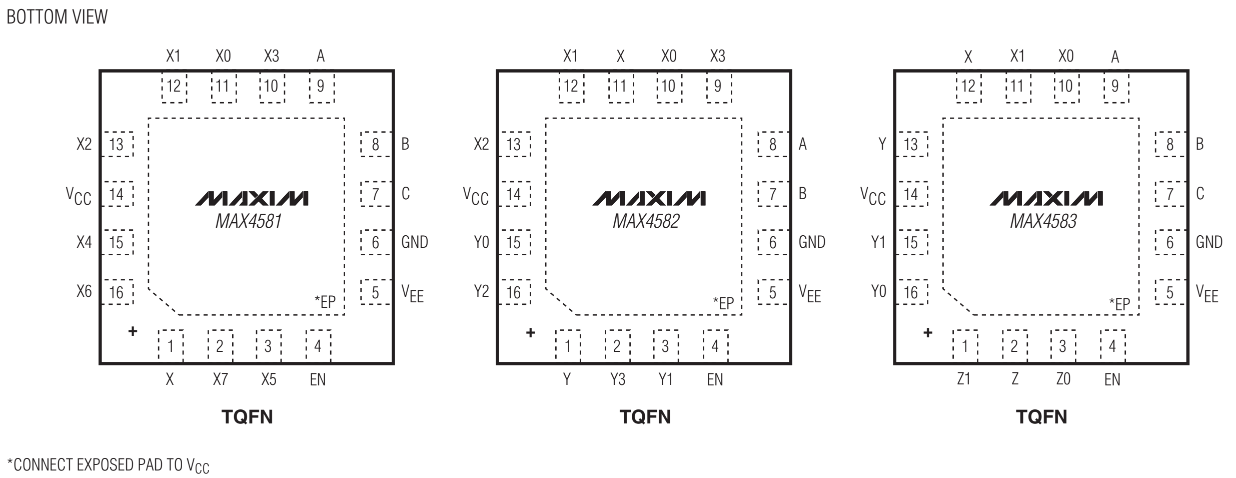


Figure 7. Capacitance

Pin Configurations/Functional Diagrams (continued)



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4581CEE+	0°C to +70°C	16 QSOP	—
MAX4581EPE+	-40°C to +85°C	16 PDIP	—
MAX4581ESE+	-40°C to +85°C	16 Narrow SO	—
MAX4581EUE+	-40°C to +85°C	16 TSSOP	—
MAX4581EEE+	-40°C to +85°C	16 QSOP	—
MAX4581ETE+	-40°C to +85°C	16 TQFN-EP*	AGH
MAX4581ASE+	-40°C to +125°C	16 Narrow SO	—
MAX4581AUE+	-40°C to +125°C	16 TSSOP	—
MAX4582CPE+	0°C to +70°C	16 PDIP	—
MAX4582CSE+	0°C to +70°C	16 Narrow SO	—
MAX4582CUE+	0°C to +70°C	16 TSSOP	—
MAX4582CEE+	0°C to +70°C	16 QSOP	—
MAX4582EPE+	-40°C to +85°C	16 PDIP	—
MAX4582ESE+	-40°C to +85°C	16 Narrow SO	—
MAX4582EUE+	-40°C to +85°C	16 TSSOP	—

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V Denotes an automotive qualified part.
T = Tape and reel.
*EP = Exposed pad.

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4582EEE+	-40°C to +85°C	16 QSOP	—
MAX4582ETE+	-40°C to +85°C	16 TQFN-EP*	AGH
MAX4582ASE+	-40°C to +125°C	16 Narrow SO	—
MAX4582AUE/V+T	-40°C to +125°C	16 TSSOP	—
MAX4583CPE+	0°C to +70°C	16 PDIP	—
MAX4583CSE+	0°C to +70°C	16 Narrow SO	—
MAX4583CUE+	0°C to +70°C	16 TSSOP	—
MAX4583CEE+	0°C to +70°C	16 QSOP	—
MAX4583EPE+	-40°C to +85°C	16 PDIP	—
MAX4583ESE+	-40°C to +85°C	16 Narrow SO	—
MAX4583EUE+	-40°C to +85°C	16 TSSOP	—
MAX4583EEE+	-40°C to +85°C	16 QSOP	—
MAX4583ETE+	-40°C to +85°C	16 TQFN–EP*	AGH
MAX4583ASE+	-40°C to +125°C	16 Narrow SO	—
MAX4583AUE+	-40°C to +125°C	16 TSSOP	—

Chip Information

PROCESS: BICMOS

TRANSISTOR COUNT: 219

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 PDIP	P16+1	**21-0043**	—
16 Narrow SO	S16+1	**21-0041**	**90-0097**
16 TSSOP	U16+2	**21-0066**	**90-0117**
16 QSOP	E16+4	**21-0055**	**90-0167**
16 TQFN	T1633+5	**21-0136**	**90-0032**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
5	6/07	Various changes	—
6	3/12	Updated TQFN, PDIP, and lead-free packaging options; updated temperature ranges	1–7, 15, 16